CLAIMS

I/We claim:

[c1] 1. A pixel sensor cell comprising:

a pinned photodiode formed in a Pwell that is formed in an N-type semiconductor substrate;

a transfer transistor placed between the pinned photodiode and an output node;

a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

an output transistor, the gate of the output transistor being coupled to the output node.

[c2] 2. The pixel sensor cell of Claim 1 wherein said transfer transistor is a depletion mode MOSFET.

[c3] 3. The pixel sensor cell of Claim 1, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

[c4] 4. The pixel sensor cell of Claim 2, further including a negative voltage generator that generates a negative voltage sufficient to turn off said depletion mode transfer transistor.

[c5] 5. The pixel sensor cell of Claim 2, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

[c6] 6. The pixel sensor cell of Claim 2, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 volts or less.

[c7] 7. A CMOS image sensor comprising:

a plurality of active pixels arranged in rows and columns formed in an N-type semiconductor substrate, at least one of said active pixels comprising:

(a) a pinned photodiode;

(b) a transfer transistor placed between the pinned photodiode and an output node, the transfer transistor being a depletion mode MOSFET; and

(c) a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

(d) an output transistor, the gate of the output transistor being coupled to the output node.;

a negative charge pump for generating a negative voltage and formed in said N-type semiconductor substrate;

a processing circuit for receiving the output of said active pixels formed in said N-type semiconductor substrate; and

an I/O circuit formed in said N-type semiconductor substrate for outputting the output of said active pixels off of said CMOS image sensor.

[c8] 8. The image sensor of Claim 7, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

[c9] 9. The image sensor of Claim 7, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

[c10] 10. The image sensor of Claim 7, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 or less volts.

[c11] 11. A CMOS image sensor comprising:

a plurality of active pixels arranged in rows and columns formed in an N-type semiconductor substrate, at least one of said active pixels comprising:

(a) a pinned photodiode;

(b) a transfer transistor placed between the pinned photodiode and an output node; and

(c) a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

(d) an output transistor, the gate of the output transistor being coupled to the output node.;

a negative charge pump for generating a negative voltage and formed in said N-type semiconductor substrate;

a processing circuit for receiving the output of said active pixels formed in said N-type semiconductor substrate; and

an I/O circuit formed in said N-type semiconductor substrate for outputting the output of said active pixels off of said CMOS image sensor.

[c12] 12. The image sensor of Claim 11 wherein said transfer transistor is a depletion mode MOSFET.

[c13] 13. The image sensor of Claim 11, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

[c14] 14. The image sensor of Claim 12, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

[c15] 15. The image sensor of Claim 12, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 or less volts.